Claims

What is claimed is:

1. A method of transforming a first topology to a reduced topology, said first topology

representing an abstraction of one or more objects, said first topology further comprising a

plurality of inter-connected elements, said method comprising the steps of:

    (a) identifying one or more elements;

    (b) analyzing the effect of reducing one or more of said identified elements on the

topological and physical characteristics of said one or more objects, and

    (c) if the effect is negligible, generating a second topology reflecting the reduction of one or

more identified elements.

2. The method of claim 1, further comprising the step of

    (d) recursively executing steps (a)-(c) until no further reduction is possible.

3. The method of claim 2, wherein the second topology is a reduced topology.

4. The method of claim 1, wherein step (a) further comprises the step of

    producing a topological approximation of the first topology.

5. The method of claim 4, wherein the topological approximation is a minimum spanning

tree (MST).

6. The method of claim 1, wherein step (a) further comprises the step of

    identifying one or more symmetric nodes from a single input tree structure.

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7. The method of claim 6, wherein step (a) further comprises the step of

identifying one or more symmetric nodes in a top-down fashion from the single input tree

structure.

8. A method of transforming a circuit from a first topology to a reduced topology, said first

topology comprising a plurality of inter-connected circuit elements, said method comprising

the steps of:

(a) identifying one or more circuit elements;

(b) analyzing the effect of reducing one or more of said identified circuit elements on the

topological and physical characteristics of said circuit; and

(c) if the effect satisfies a first predefined standard, generating a second topology reflecting

the reduction of one or more identified circuit elements.

9. The method of claim 8, further comprising the step of

(d) recursively executing steps (a)-(c) until no further reduction is possible.

10. The method of claim 9, further comprising the steps of:

(e) replacing the first predefined standard with a second predefined standard; and,

(f) repeating steps (a)-(d) for the reduced topology using the second predefined standard.

11. The method of claim 10, wherein the second predefined standard is a more relaxed

standard than the first predefined standard.

12. The method of claim 8, wherein step (a) further comprises the step of producing a

topological approximation of the first topology.

13. The method of claim 12, wherein the topological approximation is a minimum spanning tree (MST).

5   14. The method of claim 13, wherein step (a) further comprises the step of identifying one or more circuit elements from the MST, the value of each said one or more circuit elements is less than a threshold value.

15. The method of claim 8, wherein step (b) further comprises the step of analyzing the
10   variation of one or more delay measurements.

16. The method of claim 15, wherein the one or more delay measurements comprise Elmore delays.

15   17. The method of claim 14, wherein step (c) further comprises the step of eliminating the one or more circuit elements whose value is less than a threshold value.

18. The method of claim 8, wherein step (a) further comprises the step of identifying one or more circuit elements having coupling effect.
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19. The method of claim 18, wherein step (b) further comprises the steps of:
       producing a first regional topology approximating the effect of eliminating one or more circuit elements having coupling effect;
       identifying one or more crossly-coupled nodes within the first regional topology;
25   estimating the coupling effects of each said one or more crossly-coupled nodes; and

generating a second regional topology replacing the cross-coupling of each crossly-coupled node with its estimated coupling effects.

20. The method of claim 8, wherein step (a) further comprises the step of identifying one or more clusters of circuit elements.

21. The method of claim 20, wherein step (b) further comprises the steps of

determining one or more center nodes for one or more clusters; and,

analyzing the effect of moving the connection of one or more circuit elements connected

to one or more nodes within one or more said clusters to one or more said center nodes.

22. The method of claim 8, wherein step (a) further comprises the step of

identifying one or more circuit elements having similar input-output characteristics.

23. The method of claim 22, wherein step (c) further comprises the step of

merging one or more of said circuit elements having similar input-output characteristics

into one equivalent circuit element.

24. The method of claim 8, wherein step (a) further comprises the step of

identifying one or more candidate nodes including one or more quick nodes,

wherein said one or more candidates do not include any node having a capacitor directly

connected to an input node.

25. The method of claim 24, wherein step (c) further comprises the step of

eliminating one or more candidate nodes only if its degree of connectivity is equal to two.

26. The method of claim 24, wherein step (b) further comprises the steps of:

producing a regional topology approximating the effect of eliminating one or more of said candidate nodes; and,

determining, based on the regional topology, the difference in the number of circuit elements connected between two or more neighboring nodes of one or more of said candidate nodes, before and after eliminating one or more of said candidate nodes.

27. The method of claim 26, wherein step (c) further comprises the step of

eliminating one or more of said candidate notes, if the regional topology produces less number of circuit elements connected between two or more neighboring nodes of one or more of said candidate nodes.

28. The method of claim 24, wherein step (b) further comprises the step of

determining if the topology after eliminating one or more of said candidate nodes contains a voltage divider structure.

29. The method of claim 28, wherein step (c) further comprises the step of

eliminating said one or more candidate nodes if the topology after eliminating one or more of said candidate nodes does not contain a voltage divider structure.

30. The method of claim 8, wherein step (a) further comprises the step of

identifying a regional topology comprising two nodes N_1 and N_2 connected to a common node N_a, wherein N_1 is connected to N_a through resistance R_1, N_2 is connected to N_a through resistance R_2, N_1 and N_2 further having capacitance C_1 and C_2, respectively, connected to either the ground or another common node, and wherein there is no other

5   resistor connection to N_1 or N2.

31. The method of claim 30, wherein step (c) further comprises the step of

merging N_1 and N_2, if (i) the value of R_1*C_1 is approximately equal to the value of R_2*C_2, and (ii) if N_1 and N_2 are connected to additional common nodes N_{b1}, N_{b2},...,N_{bn} via

10   capacitors C_{c11}, C_{c12}, ...C_{c1n} and C_{c21}, C_{c22}, ...C_{c2n}, respectively, the value of R_1*Cc_{1i} is

approximately equal to the value of R_2*Cc_{2i}, for i=1...n.

32. The method of claim 12, wherein step (a) further comprises the step of

identifying one or more symmetric nodes.

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33. The method of claim 32, wherein step (c) further comprises the step of

merging said one or more symmetric nodes.

34. The method of claim 8, wherein the plurality of circuit elements comprise resistors and

20   capacitors.

35. The method of claim 18 or 19, wherein the one or more circuit elements having coupling

effect comprise one or more coupling capacitors.

36. The method of claim 21, wherein the one or more circuit elements connected to one or more nodes within one or more said clusters comprise one or more coupling capacitors.

37. The method of claim 28 or 29, wherein the voltage divider structure comprises two or more capacitors connected in series.

38. The method of claim 8, wherein the first topology comprises more than 100 nodes.

39. A programmed computer system for transforming a first topology to a reduced topology, said first topology representing an abstraction of one or more objects, said first topology further comprising a plurality of inter-connected elements, said programmed computer system comprising at least one memory having at least one region storing computer executable program code and at least one processor for executing the program code stored in said memory, wherein the program code comprises:

(a) code to identify one or more elements;

(b) code to analyze the effect of reducing one or more of said identified elements on the topological and physical characteristics of said one or more objects, and

(c) code to generate a second topology reflecting the reduction of one or more identified elements, if the effect is negligible.

40. The system of claim 39, wherein the program code further comprises code to recursively executing (a), (b) and (c) until no further reduction is possible.

41. The system of claim 40, wherein the second topology is a reduced topology.

42. The system of claim 39, wherein the program code further comprises code to produce a topological approximation of the first topology.

43. The system of claim 42, wherein the topological approximation is a minimum spanning tree (MST).

44. The system of claim 43, wherein the program code further comprises code to identify one or more symmetric nodes.

45. The system of claim 44, wherein the program code further comprises code to identify one or more elements of small-value from the MST.

46. The system of claim 39, wherein the plurality of inter-connected elements comprise a plurality of circuit elements.

47. The system of claim 46, wherein the program code further comprises code to analyze the variation of one or more delay measurements.

48. The system of claim 46, wherein the program code further comprises code to identify one or more circuit elements having coupling effect.

49. The system of claim 48, wherein the program code further comprises:
    code to produce a first regional topology approximating the effect of eliminating one or more circuit elements having coupling effect;
    code to identify one or more crossly-coupled nodes within the first regional topology;

code to estimate the coupling effects of each said one or more crossly-coupled nodes; and

code to generate a second regional topology replacing the cross-coupling of each crossly-coupled node with its estimated coupling effects.

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50. The system of claim 46, wherein the program code further comprises code to identify one or more clusters of circuit elements.

51. The system of claim 50, wherein the program code further comprises:

10 code to determine one or more center nodes for one or more clusters; or,

code to move the connection of one or more circuit elements connected to one or more nodes within one or more said clusters to one or more said center nodes.

52. The system of claim 46, wherein the program code further comprises code to identify one

15 or more circuit elements having similar input-output characteristics.

53. The system of claim 52, wherein the program code further comprises code to merge one or more of said circuit elements having similar input-output characteristics into one equivalent circuit element.

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54. The system of claim 46, wherein the program code further comprises code to identify one or more candidate nodes including one or more quick nodes,

wherein said one or more candidates do not include any node having a capacitor directly connected to an input node.

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55. The system of claim 54, wherein the program code further comprises code to eliminate one or more candidate nodes only if its degree of connectivity is equal to two.

56. The system of claim 54, wherein the program code further comprises:

code to produce a regional topology approximating the effect of eliminating one or more of said candidate nodes; and,

code to determine, based on the regional topology, the difference in the number of circuit elements connected between two or more neighboring nodes of one or more of said candidate nodes, before and after eliminating one or more of said candidate nodes.

57. The system of claim 56, wherein the program code further comprises code to eliminate one or more of said candidate notes, if the regional topology produces less number of circuit elements connected between two or more neighboring nodes of one or more of said candidate nodes.

58. The system of claim 54, wherein the program code further comprises code to determine if the topology after eliminating one or more of said candidate nodes contains a voltage divider structure.

59. The system of claim 58, wherein the program code further comprises code to eliminate said one or more candidate nodes if the topology after eliminating one or more of said candidate nodes does not contain a voltage divider structure.

60. The system of claim 46, wherein the program code further comprises code to identify a regional topology comprising two nodes N_1 and N_2 connected to two common nodes N_a and

N_b, wherein N_1 is connected to N_a through capacitance Cc_1 and to N_b through resistance R_1, N_2 is connected to N_a through capacitance Cc_2 and to N_b through resistance R_2, N_1 and N_2 further having ground capacitance C_1 and C_2, respectively.

5   61. The system of claim 60, wherein the program code further comprises code to merge N_1 and N_2, if the value of R_1*C_1 is approximately equal to the value of R_2*C_2 and the value of R_1*Cc_1 is approximately equal to the value of R_2*Cc_2.

62. A method of reducing coupling capacitors within a circuit topology, said method

10   comprising the steps of:

identifying one or more C-blocks;

producing a first regional topology approximating the effect of eliminating one or more nodes in one or more of said C-blocks;

estimating the coupling effects of one or more crossly-coupled nodes in the first

15   regional topology; and

generating a second regional topology replacing the cross-coupling of one or more crossly-coupled nodes with the corresponding estimated coupling effects.

63. A method of transforming a circuit from a first topology to a reduced topology, said first

20   topology comprising a plurality of inter-connected circuit elements, said method comprising the steps of:

generating a tree-like topological approximation of at least one partition of the first topology;

identifying one or more circuit elements for reduction from the tree-like topological

25   approximation; and

reducing one or more of said circuit elements in a bottom-up fashion from the leaf

nodes to the root of the tree-like topological approximation.

64. The method of claim 63, wherein the at least one partition of the first topology further

5   comprises a DC net.

65. The method of claim 63, further comprising, before the step of generating, the step of:

merging one or more nodes in the first topology into a macronode.

10   66. The method of claim 63, wherein the one or more circuit elements comprises one or

more small-valued circuit elements.

67. The method of claim 63, wherein the one or more circuit elements comprises one or

more clusters.

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68. A method of reducing capacitors within a circuit topology, said method comprising the

steps of:

identifying a topology comprising a transistor drain or source node A connected to a

node B via a small resistor, said node A and node B being coupled to a node X via capacitors

20   C_1 and C_2, respectively;

moving capacitor C_1 from between nodes A and X to between nodes B and X; and

merging capacitors C_1 and C_2 into one capacitor connected between nodes B and X.

69. A method of reducing nodes within a circuit topology, said method comprising the steps

25   of:

identifying a topology comprising two nodes P_1 and P_2 satisfying the following conditions: (i) they are receiver ports with capacitor loads C_1 and C_2, respectively, (ii) they are connected to a common node A via resistances R_1 and R_2, respectively, and (iii) both $R_1 * C_1$ and $R_2 * C_2$ are small; and

5   merging nodes P_1 and P_2 into one node.

70.   Computer executable software code stored on a computer readable medium for transforming a first topology to a reduced topology, said first topology representing an abstraction of one or more objects, said first topology further comprising a plurality of inter-

10   connected elements, said software code comprises:

     (a) code to identify one or more elements;

     (b) code to analyze the effect of reducing one or more of said identified elements on the topological and physical characteristics of said one or more objects, and

     (c) code to generate a second topology reflecting the reduction of one or more identified

15   elements, if the effect is negligible.